In re Appln. of KIMATA et al.
Application No. Unassigned

10/530720 AEG 6/2/08

SPECIFICATION AMENDMENTS

Replace the paragraph beginning at page 2, line 12 with:

With reference to Figs. ~~2 and 3~~2A to 3B, details of the surge voltage occurring at the cable connection ends of the motor 2 are described. Figs. ~~2 and 3~~2A to 3B are drawings that depict line-to-line voltage waveforms at both ends of the connection cable 3 shown in Fig. 1.

Replace the paragraph beginning at page 2, line 16 with:

Fig. ~~2 (1)~~2A depicts a case where an inverter-end line-to-line voltage Vuv_inv is varied stepwise as Vdc→0→Vdc. At this time, when a pulse width in voltage change coincides with half of a resonant cycle, as shown in Fig. ~~2 (2)~~2B, a motor-end line-to-line voltage Vuv_motor becomes three times as high as the direct-current bus voltage Vdc at maximum.

Replace the paragraph beginning at page 2, line 23 with: AEG 6/2/08

Also, Fig. ~~3 (1)~~3A depicts a case where the inverter-end line-to-line voltage Vuv_inv is varied stepwise as 0→Vdc→-Vdc→0. At this time, as shown in Fig. ~~3 (2)~~3B, the motor-end line-to-line voltage Vuv_motor becomes four times as high as the direct-current bus voltage Vdc at maximum.

Replace the paragraph beginning at page 3, line 2 with:

From the description with reference to Figs. ~~2 and 3~~2A to 3B, it is known that if the pulse width in voltage change is sufficiently large, after resonance occurring due to a stepwise voltage change is attenuated, the next stepwise voltage change is applied, and therefore a surge voltage exceeding twice the direct-current bus voltage Vdc does not occur.

Replace the paragraph beginning at page 4, line 20 with:

It is an object of the present invention to solve at least the above problems in the conventional technology. An apparatus ~~according to one aspect of the present invention, which is~~ for controlling a power converter ~~in which an output voltage is controlled by a~~

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Replace the paragraph beginning at page 49, line 9 with:

Next, with reference to ~~Fig. 24~~ Figs. 24A to 24C, a method of calculating the error Err is described. In Fig. ~~24 (1)~~24A, loci A and B of magnetic flux vectors for two PWM control cycles before voltage vector adjustment are shown. The locus A is in the previous cycle, while the locus B is the current cycle. In Fig. ~~24 (2)~~24B, loci A' and B' of magnetic flux vectors after voltage vector adjustment are shown. As a result of ensuring the minimum zero-voltage-vector output time with the locus A of the magnetic flux vectors at the previous time, it becomes the locus A' with its length being shortened. Fig. ~~24 (3)~~24C is drawn by overlaying ~~(1)~~ Fig. 24A ~~and (2) of Fig. 24 each other~~ on Fig. 24B.

Replace the paragraph beginning at page 49, line ~~9~~ 19 with:

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Here, consider the case where the end point of the locus of the magnetic flux vectors before adjustment is made to agree with that after adjustment by drawing a locus as shown in the locus B' in the present PWM control cycle. As has been described in the first embodiment ~~(Fig. 10),~~ (Figs. 10A to 10C), when the voltage vectors are adjusted according to equation 3 so that the relative ratio of the output times of the voltage vectors other than the zero-voltage vectors is unchanged, a triangle of the locus A is similar to a triangle of the locus A'. Similarly, a triangle of the locus B is similar to a triangle of the locus B'.

Delete the paragraph beginning at page 51, line 7:

~~Eighth Embodiment~~

Replace the paragraph beginning at page 51, line 21 with:

That is, taking note of Fig. ~~12(1)~~12A, eliminating the zero-voltage vector V7 does not pose the line-to-line voltages Vvw and Vwu. However, as for the line-to-line voltage Vuv, two pulses of the voltage vector V1 are present over the voltage vector V2. This corresponds to the case of ~~(1-2) of Fig. 14~~ Fig. 14B, with the voltage vector V2 being replaced by the zero-voltage vector. That is, when the output time of the zero-voltage vector is adjusted to zero, depending on the non-zero-voltage-vector output time, a surge voltage may occur. In such a case, in the ~~eight~~ eighth embodiment, the concept of ensuring the minimum zero-voltage-vector output time is applied. Hereinafter, a description is ~~made~~ implied according to